What is claimed :

1. An integrated select circuit comprising:

a plurality of drain diffusion regions, each region laterally spaced apart from other drain diffusion regions;

a plurality of source diffusion regions, each region laterally spaced between a pair of drain diffusion regions of the plurality of drain diffusion regions;

a plurality of local bit lines, each local bit line coupled to a different drain diffusion region of the plurality of drain diffusion regions; and

a plurality of global bit line each coupled to a set of the plurality of source diffusion regions, wherein a first drain diffusion region is laterally wider than a second drain diffusion region such that a third local bit line can traverse between a first local bit line and a second local bit line of the plurality of local bit lines.

2. The circuit of claim 1 wherein the third local bit line is generally located above the first drain diffusion region.

3. The circuit of claim 1 further comprising:

a first gate positioned between the first drain diffusion region and a first source diffusion region of the plurality of source diffusion regions, the first gate is coupled to a first select line; and

a second gate positioned between the first source diffusion region and the second drain diffusion region, the second gate is coupled to a second select line.

4. The circuit of claim 1 wherein the device is manufactured so that the plurality of local bit lines is on a different planer level than the plurality of global bit lines.

5. The circuit of claim 4 wherein the plurality of local bit lines is formed on a first metal level and the plurality of global bit lines is formed on a second metal level.

6. The circuit of claim 1 wherein the plurality of local bit lines and the plurality of global bit lines are formed in metal layers.

7. The circuit of claim 6 wherein the plurality of global bit lines are all formed in the same metal layer.

8. An integrated select circuit comprising:

a first drain diffusion region;

a second drain diffusion region laterally spaced apart from the first drain diffusion region;

a source diffusion region laterally spaced between the first drain diffusion region and the second drain diffusion region;

a first local bit line coupled to the first drain diffusion region;

a second local bit line coupled to the second drain diffusion region; and

a global bit line coupled to the source diffusion region, wherein the first drain diffusion region is laterally wider than the second drain diffusion region such that a third local bit line can traverse between the first local bit line and the second local bit line.

9. The circuit of claim 8 wherein the first and second local bit lines are generally parallel to each other.

10. The circuit of claim 8 and further including an array of flash memory cells.

11. The circuit of claim 10 wherein the flash memory cells are floating gate memory cells.

12. The circuit of claim 10 wherein each of the flash memory cells is comprised of a floating gate capable of holding a charge.

13. The circuit of claim 12 wherein a presence or absence of the charge determines a state of the flash memory cell.

14. The circuit of claim 8 wherein there are twice as many local bit lines as global bit lines.

15. An integrated select circuit in a flash memory device, the circuit comprising:

a first drain diffusion region;

a second drain diffusion region laterally spaced apart from the first drain diffusion region;

a source diffusion region laterally spaced between the first drain diffusion region and the second drain diffusion region;

a first local bit line coupled to the first drain diffusion region;

a second local bit line coupled to the second drain diffusion region;

a global bit line coupled to the source diffusion region, wherein the first drain diffusion region is laterally wider than the second drain diffusion region such that a third local bit line can traverse between the first local bit line and the second local bit line; and

a first active area that includes the first local bit line and the global bit line.

16. The circuit of claim 15 and further including a second active area that includes the second local bit line.